1. Description

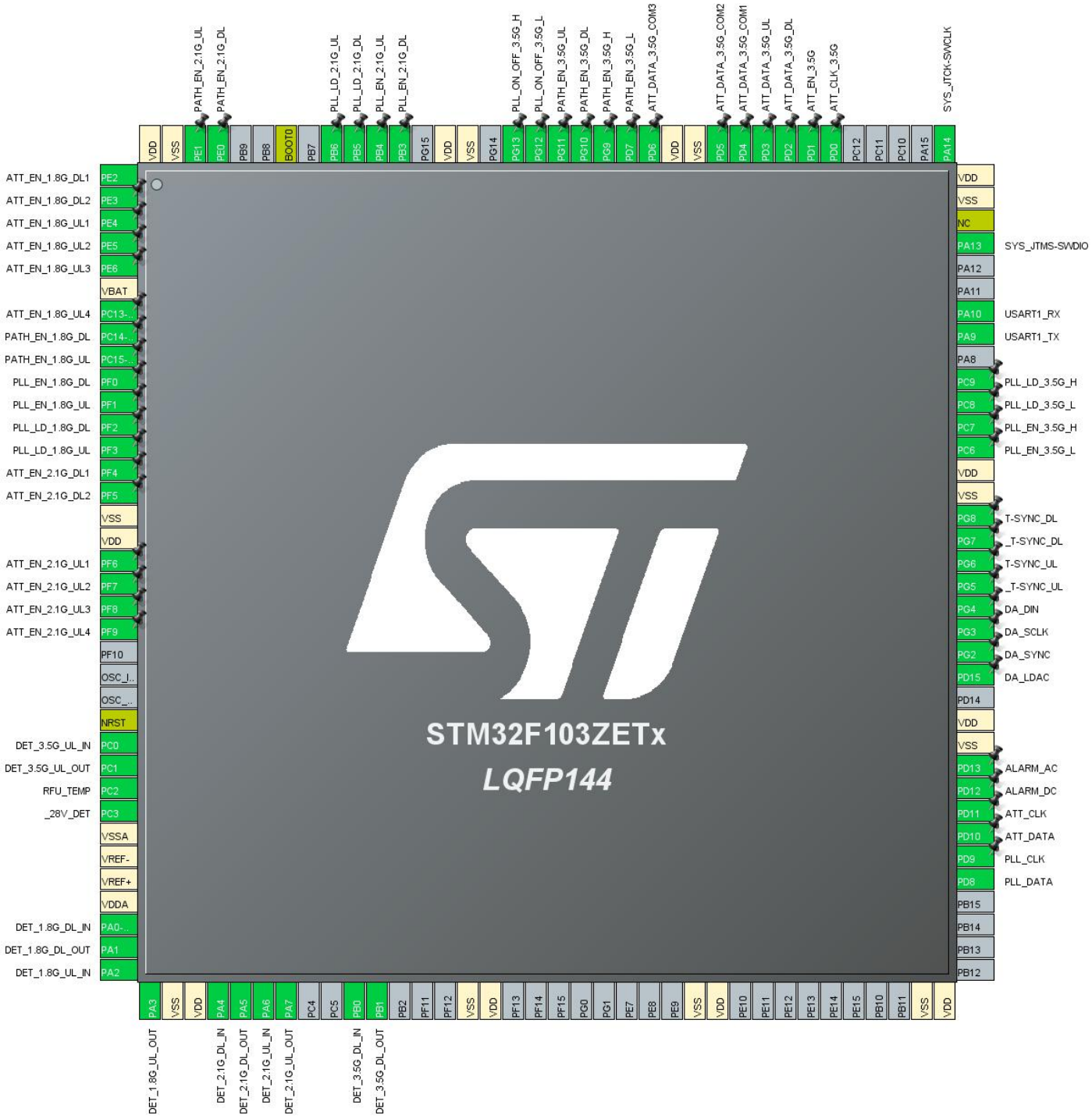
1.1. Project

Project Name	STM32F103_ATTEN_PLL_Zig
Board Name	custom
Generated with:	STM32CubeMX 5.2.1
Date	07/01/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

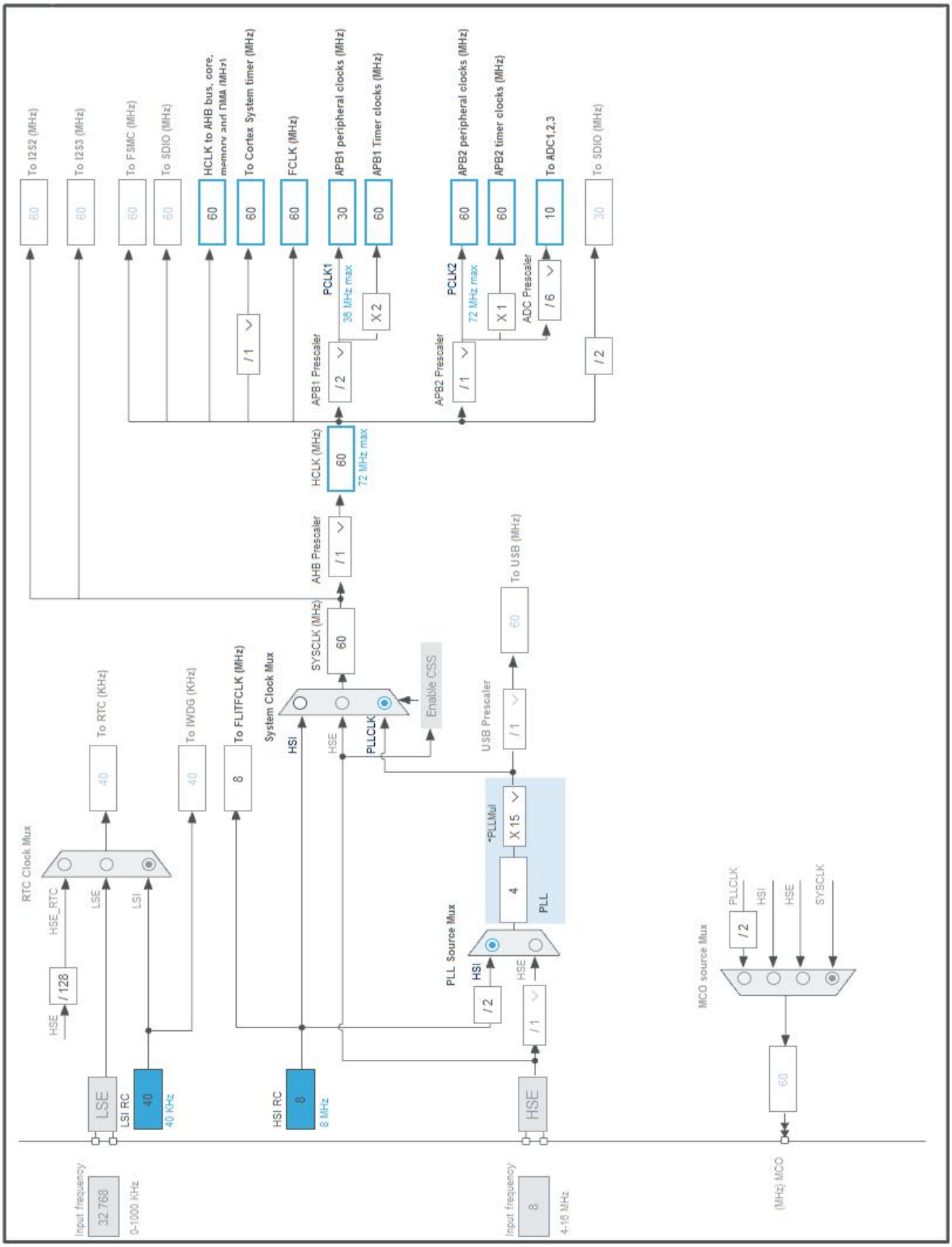
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	ATT_EN_1.8G_DL1
2	PE3 *	I/O	GPIO_Output	ATT_EN_1.8G_DL2
3	PE4 *	I/O	GPIO_Output	ATT_EN_1.8G_UL1
4	PE5 *	I/O	GPIO_Output	ATT_EN_1.8G_UL2
5	PE6 *	I/O	GPIO_Output	ATT_EN_1.8G_UL3
6	VBAT	Power		
7	PC13-TAMPER-RTC *	I/O	GPIO_Output	ATT_EN_1.8G_UL4
8	PC14-OSC32_IN *	I/O	GPIO_Output	PATH_EN_1.8G_DL
9	PC15-OSC32_OUT *	I/O	GPIO_Output	PATH_EN_1.8G_UL
10	PF0 *	I/O	GPIO_Output	PLL_EN_1.8G_DL
11	PF1 *	I/O	GPIO_Output	PLL_EN_1.8G_UL
12	PF2 *	I/O	GPIO_Input	PLL_LD_1.8G_DL
13	PF3 *	I/O	GPIO_Input	PLL_LD_1.8G_UL
14	PF4 *	I/O	GPIO_Output	ATT_EN_2.1G_DL1
15	PF5 *	I/O	GPIO_Output	ATT_EN_2.1G_DL2
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	ATT_EN_2.1G_UL1
19	PF7 *	I/O	GPIO_Output	ATT_EN_2.1G_UL2
20	PF8 *	I/O	GPIO_Output	ATT_EN_2.1G_UL3
21	PF9 *	I/O	GPIO_Output	ATT_EN_2.1G_UL4
25	NRST	Reset		
26	PC0	I/O	ADC1_IN10	DET_3.5G_UL_IN
27	PC1	I/O	ADC1_IN11	DET_3.5G_UL_OUT
28	PC2	I/O	ADC1_IN12	RFU_TEMP
29	PC3	I/O	ADC1_IN13	_28V_DET
30	VSSA	Power		
31	VREF-	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	ADC1_IN0	DET_1.8G_DL_IN
35	PA1	I/O	ADC1_IN1	DET_1.8G_DL_OUT
36	PA2	I/O	ADC1_IN2	DET_1.8G_UL_IN
37	PA3	I/O	ADC1_IN3	DET_1.8G_UL_OUT
38	VSS	Power		
39	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PA4	I/O	ADC1_IN4	DET_2.1G_DL_IN
41	PA5	I/O	ADC1_IN5	DET_2.1G_DL_OUT
42	PA6	I/O	ADC1_IN6	DET_2.1G_UL_IN
43	PA7	I/O	ADC1_IN7	DET_2.1G_UL_OUT
46	PB0	I/O	ADC1_IN8	DET_3.5G_DL_IN
47	PB1	I/O	ADC1_IN9	DET_3.5G_DL_OUT
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
77	PD8 *	I/O	GPIO_Output	PLL_DATA
78	PD9 *	I/O	GPIO_Output	PLL_CLK
79	PD10 *	I/O	GPIO_Output	ATT_DATA
80	PD11 *	I/O	GPIO_Output	ATT_CLK
81	PD12 *	I/O	GPIO_Input	ALARM_DC
82	PD13 *	I/O	GPIO_Input	ALARM_AC
83	VSS	Power		
84	VDD	Power		
86	PD15 *	I/O	GPIO_Output	DA_LDAC
87	PG2 *	I/O	GPIO_Output	DA_SYNC
88	PG3 *	I/O	GPIO_Output	DA_SCLK
89	PG4 *	I/O	GPIO_Output	DA_DIN
90	PG5 *	I/O	GPIO_Output	_T-SYNC_UL
91	PG6 *	I/O	GPIO_Output	T-SYNC_UL
92	PG7 *	I/O	GPIO_Output	_T-SYNC_DL
93	PG8 *	I/O	GPIO_Output	T-SYNC_DL
94	VSS	Power		
95	VDD	Power		
96	PC6 *	I/O	GPIO_Output	PLL_EN_3.5G_L
97	PC7 *	I/O	GPIO_Output	PLL_EN_3.5G_H
98	PC8 *	I/O	GPIO_Input	PLL_LD_3.5G_L
99	PC9 *	I/O	GPIO_Input	PLL_LD_3.5G_H
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	NC	NC		
107	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
114	PD0 *	I/O	GPIO_Output	ATT_CLK_3.5G
115	PD1 *	I/O	GPIO_Output	ATT_EN_3.5G
116	PD2 *	I/O	GPIO_Output	ATT_DATA_3.5G_DL
117	PD3 *	I/O	GPIO_Output	ATT_DATA_3.5G_UL
118	PD4 *	I/O	GPIO_Output	ATT_DATA_3.5G_COM1
119	PD5 *	I/O	GPIO_Output	ATT_DATA_3.5G_COM2
120	VSS	Power		
121	VDD	Power		
122	PD6 *	I/O	GPIO_Output	ATT_DATA_3.5G_COM3
123	PD7 *	I/O	GPIO_Output	PATH_EN_3.5G_L
124	PG9 *	I/O	GPIO_Analog	PATH_EN_3.5G_H
125	PG10 *	I/O	GPIO_Output	PATH_EN_3.5G_DL
126	PG11 *	I/O	GPIO_Output	PATH_EN_3.5G_UL
127	PG12 *	I/O	GPIO_Output	PLL_ON_OFF_3.5G_L
128	PG13 *	I/O	GPIO_Output	PLL_ON_OFF_3.5G_H
130	VSS	Power		
131	VDD	Power		
133	PB3 *	I/O	GPIO_Output	PLL_EN_2.1G_DL
134	PB4 *	I/O	GPIO_Output	PLL_EN_2.1G_UL
135	PB5 *	I/O	GPIO_Input	PLL_LD_2.1G_DL
136	PB6 *	I/O	GPIO_Input	PLL_LD_2.1G_UL
138	BOOT0	Boot		
141	PE0 *	I/O	GPIO_Output	PATH_EN_2.1G_DL
142	PE1 *	I/O	GPIO_Output	PATH_EN_2.1G_UL
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32F103_ATTEN_PLL_Zig
Project Folder	D:\workspace\STM32F103_ATTEN_PLL_Zig
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F1 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103ZETx
Datasheet	14611_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN3

mode: IN4

mode: IN5

mode: IN6

mode: IN7

mode: IN8

mode: IN9

mode: IN10

mode: IN11

mode: IN12

mode: IN13

7.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	**14 ***
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**2 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**3 ***
Channel	Channel 0

Sampling Time	1.5 Cycles
Rank	**4 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**5 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**6 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**7 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**8 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**9 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**10 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**11 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**12 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**13 ***
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**14 ***
Channel	Channel 0
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. RCC

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. USART1

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	n/a	n/a	DET_3.5G_UL_IN
	PC1	ADC1_IN11	Analog mode	n/a	n/a	DET_3.5G_UL_OUT
	PC2	ADC1_IN12	Analog mode	n/a	n/a	RFU_TEMP
	PC3	ADC1_IN13	Analog mode	n/a	n/a	_28V_DET
	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	DET_1.8G_DL_IN
	PA1	ADC1_IN1	Analog mode	n/a	n/a	DET_1.8G_DL_OUT
	PA2	ADC1_IN2	Analog mode	n/a	n/a	DET_1.8G_UL_IN
	PA3	ADC1_IN3	Analog mode	n/a	n/a	DET_1.8G_UL_OUT
	PA4	ADC1_IN4	Analog mode	n/a	n/a	DET_2.1G_DL_IN
	PA5	ADC1_IN5	Analog mode	n/a	n/a	DET_2.1G_DL_OUT
	PA6	ADC1_IN6	Analog mode	n/a	n/a	DET_2.1G_UL_IN
	PA7	ADC1_IN7	Analog mode	n/a	n/a	DET_2.1G_UL_OUT
	PB0	ADC1_IN8	Analog mode	n/a	n/a	DET_3.5G_DL_IN
	PB1	ADC1_IN9	Analog mode	n/a	n/a	DET_3.5G_DL_OUT
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_1.8G_DL1
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_1.8G_DL2
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_1.8G_UL1
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_1.8G_UL2
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_1.8G_UL3
	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_1.8G_UL4
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_1.8G_DL
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_1.8G_UL
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_EN_1.8G_DL
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_EN_1.8G_UL
	PF2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_LD_1.8G_DL
	PF3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_LD_1.8G_UL

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_2.1G_DL1
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_2.1G_DL2
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_2.1G_UL1
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_2.1G_UL2
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_2.1G_UL3
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_2.1G_UL4
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_DATA
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_CLK
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_DATA
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_CLK
	PD12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ALARM_DC
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ALARM_AC
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DA_LDAC
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DA_SYNC
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DA_SCLK
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DA_DIN
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	_T-SYNC_UL
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	T-SYNC_UL
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	_T-SYNC_DL
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	T-SYNC_DL
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_EN_3.5G_L
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_EN_3.5G_H
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_LD_3.5G_L
	PC9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_LD_3.5G_H
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_CLK_3.5G
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_EN_3.5G
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_DATA_3.5G_DL
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_DATA_3.5G_UL
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_DATA_3.5G_COM1
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_DATA_3.5G_COM2
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ATT_DATA_3.5G_COM3
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_3.5G_L
	PG9	GPIO_Analog	Analog mode	n/a	n/a	PATH_EN_3.5G_H
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_3.5G_DL
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_3.5G_UL
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_ON_OFF_3.5G_L
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_ON_OFF_3.5G_H
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_EN_2.1G_DL
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_EN_2.1G_UL
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_LD_2.1G_DL

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_LD_2.1G_UL
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_2.1G_DL
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PATH_EN_2.1G_UL

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		

*** User modified value**

9. Software Pack Report